IN THE CLAIMS

1. (Currently Amended) A process for fabricating an integrated circuit, comprising:

producing several metallization levels, two of which are mutually separated by an interlevel insulating layer; ~~layers;~~

producing intertrack insulating layers each separating tracks of the same metallization level; and

producing at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the production of the at least one capacitor comprises:

simultaneously producing, in at least part of an intertrack insulating layer associated with one of the several metallization levels, ~~a particular metallization level,~~ on the one hand, the lower electrode, the upper electrode, and the dielectric layer of the at least one capacitor and, on the other hand, simultaneously producing a conducting trench which laterally extends the lower electrode of the at least one capacitor, and is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the at least one capacitor; and

producing, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads which come into contact with the upper electrode of the at least one capacitor and with the conducting trench, respectively.

2. (Currently Amended) The process according to Claim 1, wherein the conducting trench comprises ~~only the~~ a conducting material forming the lower electrode.

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3. (Currently Amended) The process according to Claim 1, wherein the tracks of one of the several metallization levels ~~a particular metallization level~~ are produced simultaneously with the formation of the upper electrode of the at least one capacitor.

4. (Currently Amended) The process according to Claim 1, wherein the producing ~~production~~ of the the at least one capacitor and of the conducting trench comprises:

a) forming one of the intertrack insulating layers ~~formation of the intertrack insulating layer~~ on ~~an~~ the interlevel insulating layer;

b) etching at least part of the one of the intertrack insulating layers ~~intertrack insulating layer so as~~ to form a cavity having a main part laterally extended by the conducting trench;

c) ~~formation of~~ forming a first conducting layer of a first conducting material in the cavity and the conducting trench ~~on the structure~~ obtained in step b) and forming ~~formation of~~ a dielectric layer of a dielectric material on the first conducting layer;

d~~) formation of~~ forming a second conducting layer of a second conducting material on the dielectric layer ~~so as~~ to fill the main part of the cavity, wherein the dimensions of the conducting trench and the thickness of the first conducting layer and of the dielectric layer being chosen ~~so as~~ to obtain, after step d), ~~a~~ the conducting trench comprising at least the first conducting material but not containing the second conducting material; and

e) chemical-mechanical polishing ~~of the multilayer stack formed in steps c) and d) so as to leave,~~ the first conducting layer, the dielectric layer, and the second conducting layer, to form the at least one capacitor in the main part of the cavity, ~~the capacitor whose~~

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wherein the lower electrode is formed from a residual part of the first conducting layer ~~coating of~~ resided in internal walls of the cavity and ~~whose~~ the upper electrode is formed from a residual part of the second conducting layer, which is separated from the residual part of the first conducting layer by a residual part of the dielectric layer; and to leave another ~~, and to leave, in the trench, another~~ residual part of the first conducting layer ~~coating of at least internal walls of~~ in the conducting trench. ~~, to the exclusion of any residual part of the second layer.~~

5. (Currently Amended) The process according to Claim 4, wherein the conducting trench comprises material of ~~only~~ the first conducting layer ~~material~~ forming the lower electrode.

6. (Currently Amended) The process according to Claim 4, wherein the tracks of ~~a particular metallization level~~ one of the several metallization levels are produced simultaneously with the producing ~~formation~~ of the upper electrode of the at least one capacitor.

7. (Currently Amended) The process according to Claim 4, wherein the producing ~~production~~ of the tracks of ~~a particular metallization level~~ one of the several metallization levels comprises:

after step c), etching the dielectric layer of the first conducting layer and of the intertrack insulating layer ~~so as~~ to form at least one auxiliary trench;

the formation of the second conducting layer being carried out in step d) ~~so as~~ to

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substantially fill the conducting trench; and

~~the~~ chemical-mechanical polishing ~~being carried out in step c) so as~~ to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

8. (Currently Amended) The process according to Claim 4, wherein the first conducting layer and the dielectric layer are formed in step c) by a conformal coating and in that the width of the conducting trench is at least twice the thickness of the first conducting layer and less than twice the sum of the thickness of the first conducting layer and of the thickness of the dielectric layer.

9. (Currently Amended) The process according to Claim 8, wherein the conducting trench comprises material of ~~only~~ the first conducting layer ~~material~~ forming the lower electrode.

10. (Currently Amended) The process according to Claim 8, wherein the tracks of a ~~particular metallization level~~ one of the several metallization levels are produced simultaneously with the producing ~~formation~~ of the upper electrode of the at least one capacitor.

11. (Currently Amended) The process according to Claim 10, wherein the producing ~~production~~ of the tracks of ~~a particular metallization level~~ one of the several metallization levels comprises:

after step c), etching of the dielectric layer, of the first conducting layer and of the

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intertrack insulating layer ~~so as~~ to form at least one auxiliary trench;

the ~~deposition~~ formation of the second conducting layer being carried out in step d) ~~so as~~ to substantially fill the conducting trench ~~or trenches~~; and

~~the~~ chemical-mechanical polishing ~~carried out in step e) so as~~ to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

12. (Currently Amended) An integrated circuit comprising:

several metallization levels, which are mutually separated by interlevel insulating layers; ~~, and~~

intertrack insulating layers each separating the tracks of the same metallization level; ~~, and~~

at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the at least one capacitor is located in at least part of an intertrack insulating layer associated with one of the several metallization levels, ~~a particular metallization level, in that~~ the lower electrode of the at least one capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and one of ~~in that the integrated circuit comprises, in~~ the interlevel insulating layers ~~layer~~ covering the intertrack insulating layer; and ;

two conducting pads which come into contact with the upper electrode of the at least one capacitor and with the conducting trench, respectively.

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13. (Currently Amended) The integrated circuit according to Claim 12, wherein the tracks of one of the several metallization levels ~~a particular metallization level~~ are formed from the material as that forming the upper electrode of the at least one capacitor.

14. (Currently Amended) The integrated circuit according to Claim 12, wherein the conducting trench comprises ~~only~~ the conducting material forming the lower electrode.

15. (Currently Amended) The integrated circuit according to Claim 14, wherein the tracks of one of the several metallization levels ~~a particular metallization level~~ are formed from the material as that forming the upper electrode of the at least one capacitor.

16. (Currently Amended) The integrated circuit according to Claim 12, wherein the conducting trench comprises ~~only the~~ dielectric encapsulated by ~~the~~ a conducting material forming the lower electrode.

17. (Currently Amended) The integrated circuit according to Claim 16, wherein the tracks of one of the several metallization levels ~~a particular metallization level~~ are formed from the material as that forming the upper electrode of the capacitor.

18. (Currently Amended) An integrated circuit comprising:

a plurality of metallization levels that are mutually separated by interlevel insulating layers; ~~, and~~

a plurality of intertrack insulating layers, each of the plurality of intertrack insulating layers separating the tracks of the same metallization level; and

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at least one capacitor comprising a lower electrode and an upper electrode, which are mutually separated by a dielectric layer, and wherein the capacitor is located in at least part of an intertrack insulating layer associated with one of the plurality of metallization levels ~~a particular metallization level~~, and ~~in that~~ the lower electrode of the at least one capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the at least one capacitor, and ~~wherein, in~~ the interlevel insulating layer covering the intertrack insulating layer; and ;

two conducting pads ~~come into~~ being in contact with the upper electrode of the capacitor and with the conducting trench, respectively, and wherein the tracks of one of the plurality of metallization levels ~~the particular metallization level~~ are formed from the same material as that of ~~forming~~ the upper electrode of the at least one capacitor.

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